IN THE CLAIMS

1-9 (Cancelled)

10. (Previously Presented) A latch circuit, comprising:

a pair of cross-coupled amplifiers, wherein each amplifier includes:

a first transistor of a first conductivity type;

a dual-gated metal-oxide semiconducting field effect transistor (MOSFET) of a second conductivity type, wherein a drain region for the dual-gated MOSFET is coupled to a drain region of the first transistor in the same amplifier, is coupled directly to a gate of the first transistor of the first conductivity type in the other amplifier in the pair of cross-coupled amplifiers, and is coupled to a gate of the dual-gated MOSFET in the other amplifier in the pair of cross-coupled amplifiers, the dual-gated MOSFET having a threshold voltage ranging from about 0.3 V to about 0.35V;

a pair of input transmission lines, wherein each one of the pair of input transmission lines is coupled to another gate of the dual-gated MOSFET in each amplifier, the pair of input transmission lines directly coupling the another gate in each amplifier external to the latch circuit; and

a pair of output transmission lines, wherein each one of the pair of output transmission lines is coupled to the drain region of the first transistor and to the drain region of the dual-gated MOSFET.

11. (Previously Presented) The latch circuit of claim 10, wherein the first transistor includes a p-channel metal oxide semiconductor (PMOS) transistor, and wherein the dual-gated MOSFET include n-channel metal oxide semiconductor (NMOS) transistors.

12. (Cancelled)

13. (Original) The latch circuit of claim 10, wherein the pair of input transmission lines are bit lines and wherein the bit line capacitances are removed from the pair of output transmission lines.

14. (Original) The latch circuit of claim 13, wherein each bit line is coupled to a number of memory cells in an array of memory cells.

15. (Original) The latch circuit of claim 10, wherein the latch circuit is coupled to a power supply voltage of less than 1.0 Volts.

16. (Previously Presented) A latch circuit, comprising:

a pair of cross-coupled amplifiers, wherein each amplifier includes:

a first transistor of a first conductivity type;

a dual-gated metal-oxide semiconducting field effect transistor (MOSFET) of a second conductivity type, wherein a drain region for the dual-gated MOSFET is coupled to a drain region of the first transistor in the same amplifier, is coupled directly to a gate of the first transistor of the first conductivity type in the other amplifier in the pair of cross-coupled amplifiers, and is coupled to a gate of the dual-gated MOSFET in the other amplifier in the pair of cross-coupled amplifiers;

a pair of input transmission lines, wherein each one of the pair of input transmission lines is coupled to another gate of the dual-gated MOSFET in each amplifier, the pair of input transmission lines directly coupling the another gate in each amplifier external to the latch circuit; and

a pair of output transmission lines, wherein each one of the pair of output transmission lines is coupled to the drain region of the first transistor and to the drain region of the dual-gated MOSFET, wherein the latch circuit is able to output a full output sense voltage in less than 10 nanoseconds (ns).

17. (Previously Presented) An amplifier circuit, comprising:

a pair of cross-coupled inverters, wherein each inverter includes:

a transistor of a first conductivity type;

a dual-gated metal-oxide semiconducting field effect transistor (MOSFET) of a second conductivity type, wherein the transistor of a first conductivity type in each inverter and the a dual-gated MOSFET are coupled at a drain region in the same inverter, and wherein the drain region in each inverter is further coupled directly to a gate of the transistor of the first conductivity type in the other inverter of the pair of cross-couple inverters, and is coupled to one gate of the dual-gated MOSFET in the other inverter of the pair of cross-couple inverters, the dual-gated MOSFET having a threshold voltage ranging from about 0.3 V to about 0.35V;

a pair of input transmission lines, wherein each one of the pair of input transmission lines is coupled to another gate of the dual-gated MOSFET in each inverter respectively, the pair of input transmission lines directly coupling the another gate in each amplifier external to the latch circuit; and

a pair of output transmission lines, wherein each one of the pair of output transmission lines is coupled to the drain region on each one of the pair of cross-coupled inverters.

18. (Previously Presented) The amplifier circuit of claim 17, wherein the transistor of a first conductivity type includes a p-channel metal oxide semiconductor (PMOS) transistor, and wherein the dual-gated MOSFET of a second conductivity type is divided into two separate n-channel metal oxide semiconductor (NMOS) transistors each driven by one of the dual gates.

19. (Cancelled)

20. (Original) The amplifier circuit of claim 17, wherein the pair of cross-coupled inverters comprise a sense amplifier, and wherein the sense amplifier is included in a memory circuit.

21. (Original) The amplifier circuit of claim 20, wherein the sense amplifier is coupled to a power supply voltage of less than 1.0 Volts.

22. (Previously Presented) An amplifier circuit, comprising:

a pair of cross-coupled inverters, wherein each inverter includes:

a transistor of a first conductivity type;

a dual-gated metal-oxide semiconducting field effect transistor (MOSFET) of a second conductivity type, wherein the transistor of a first conductivity type in each inverter and the a dual-gated MOSFET are coupled at a drain region in the same inverter, and wherein the drain region in each inverter is further coupled directly to a gate of the transistor of the first conductivity type in the other inverter of the pair of cross-couple inverters, and is coupled to one gate of the dual-gated MOSFET in the other inverter of the pair of cross-couple inverters;

a pair of input transmission lines, wherein each one of the pair of input transmission lines is coupled to another gate of the dual-gated MOSFET in each inverter respectively, the pair of input transmission lines directly coupling the another gate in each amplifier external to the latch circuit; and

a pair of output transmission lines, wherein each one of the pair of output transmission lines is coupled to the drain region on each one of the pair of cross-coupled inverters, wherein the sense amplifier is able to output a full output sense voltage in less than 10 nanoseconds (ns).

23. (Previously Presented) A memory circuit, comprising:

a number of memory arrays;

at leasc one sense amplifier, wherein the sense amplifier includes:

a pair of cross-coupled inverters, wherein each inverter includes:

a p-channel metal oxide semiconductor (PMOS) transistor; and

a dual-gate metal oxide semiconductor (NMOS) transistor wherein a drain region of the PMOS transistor in each inverter is coupled to a drain region of for the dual-gate NMOS transistor in the same inverter, is coupled directly to a gate of the PMOS transistor in the other inverter of the pair of cross-couple inverters, and to one gate of the dual-gate NMOS transistor in the other inverter of the pair of cross-couple inverters, the dual-gated NMOS having a threshold voltage ranging from about 0.3 V to about 0.35V;

a complementary pair of bit lines coupling the at least one sense amplifier to a number of memory cells in the number of memory arrays, and wherein each one of the complementary pair of bit lines couples to another gate of the dual-gate NMOS transistor in each inverter, the complementary pair of bit lines directly coupling the another gate in each amplifier external to the sense amplifier; and

a pair of output transmission lines, wherein each one of the pair of output transmission lines is coupled to the drain region of the PMOS transistor and the drain region for the dual-gate NMOS transistor in each inverter.

24. (Original) The memory circuit of claim 23, wherein the memory circuit includes a folded bit line memory circuit.

25. (Cancelled)

26. (Original) The memory circuit of claim 23, wherein the at least one sense amplifier is coupled to a power supply voltage of less than 1.0 Volts.

27. (Original) The memory circuit of claim 23, wherein the at least one sense amplifier is able to output a full output sense voltage in less than 10 nanoseconds (ns).

28. (Original) The memory circuit of claim 23, wherein the memory circuit further includes a number of equilibration and a number of isolation transistors coupled to the complementary pair of bit lines.

29. (Previously Presented) An electronic system, comprising:

a processor;

a memory device; and

a bus coupling the processor and the memory device, the memory device further including a sense amplifier, comprising:

a pair of cross-coupled inverters, wherein each inverter includes:

a p-channel metal oxide semiconductor (PMOS) transistor; and

a dual-gate metal oxide semiconductor (NMOS) transistor having a threshold voltage ranging from about 0.3 V to about 0.35V, wherein a drain region of the PMOS transistor in each inverter is coupled to a drain region for the dual-gate NMOS transistor in the same inverter, is coupled directly to a gate of the PMOS transistor in the other inverter of the pair of cross-couple inverters, and is coupled to one gate of the dual-gate NMOS transistor in the other inverter of the pair of cross-couple inverters;

a complementary pair of bit lines coupling the at least one sense amplifier to a number of memory cells in a memory cell array, and wherein each one of the complementary pair of bit lines couples to another gate of the dual-gate NMOS transistor in each inverter, the complementary pair of bit lines directly coupling the another gate in each amplifier external to the sense amplifier; and

a pair of output transmission lines, wherein each one of the pair of output transmission lines is coupled to the drain region of the PMOS transistor and the drain region for the dual-gate NMOS transistor in each inverter.

30. (Original) The electronic system of claim 29, wherein the sense amplifier is coupled to a power supply voltage of less than 1.0 Volt.

31. (Previously Presented) An electronic system, comprising:

a processor;

a memory device; and

a bus coupling the processor and the memory device, the memory device further including a sense amplifier, comprising:

a pair of cross-coupled inverters, wherein each inverter includes:

a p-channel metal oxide semiconductor (PMOS) transistor; and

a dual-gate metal oxide semiconductor (NMOS) transistor wherein a drain region of the PMOS transistor in each inverter is coupled to a drain region for the dual-gate NMOS transistor in the same inverter, is coupled directly to a gate of the PMOS transistor in the

other inverter of the pair of cross-couple inverters, and is coupled to one gate of the dual-gate NMOS transistor in the other inverter of the pair of cross-couple inverters;

a complementary pair of bit lines coupling the at least one sense amplifier to a number of memory cells in a memory cell array, and wherein each one of the complementary pair of bit lines couples to another gate of the dual-gate NMOS transistor in each inverter, the complementary pair of bit lines directly coupling the another gate in each amplifier external to the sense amplifier; and

a pair of output transmission lines, wherein each one of the pair of output transmission lines is coupled to the drain region of the PMOS transistor and the drain region for the dual-gate NMOS transistor in each inverter, wherein the sense amplifier is able to output a full output sense voltage in less than 10 nanoseconds (ns).

32. (Previously Presented) An integrated circuit, comprising:

a processor;

a memory operatively coupled to the processor; and

wherein the processor and memory are formed on the same semiconductor substrate and the integrated circuit includes at least one sense amplifier, comprising:

a pair of cross-coupled inverters, wherein each inverter includes:

a transistor of a first conductivity type;

a dual-gate transistor of a second conductivity type wherein a drain region for the dual-gate transistor in each inverter is coupled to a drain region of the transistor of the first conductivity type in the same inverter, is coupled directly to a gate of the transistor of the first conductivity type in the other inverter of the pair of cross-couple inverters, and to one gate of the dual-gate transistor in the other inverter of the pair of cross-couple inverters, the dual-gated transistor having a threshold voltage ranging from about 0.3 V to about 0.35V;

a pair of bit lines, wherein each one of the pair of bit lines is coupled to another gate of the dual-gate transistors in each inverter, the pair of bit lines directly coupling the another gate of the dual-gate transistors in each inverter external to the sense amplifier; and

a pair of output transmission lines, wherein each one of the pair of output transmission lines is coupled to the drain region of the dual-gate transistor and the drain region of the transistor of the first conductivity type in each inverter.

33. (Previously Presented) A method for forming a current sense amplifier, comprising:
cross coupling a pair of inverters, wherein each inverter includes:
a transistor of a first conductivity type;
a dual-gate transistor of a second conductivity type wherein a drain region for the dual-gate transistor is coupled to a drain region of the transistor of the first conductivity type, the dual-gated MOSFET having a threshold voltage ranging from about 0.3 V to about 0.35V; and
coupling external to the sense amplifier one gate of each dual-gate transistor of each inverter, wherein cross coupling the pair of inverters includes directly coupling the drain region for the transistor of the first conductivity type and the drain region for the dual-gate transistor in one inverter to a gate of the transistor of a first conductivity type and to one gate of the dual-gate transistor in the other inverter.

34. (Previously Presented) The method of claim 33, wherein cross coupling the pair of inverters includes forming the first transistor of the first conductivity type as a p-channel metal oxide semiconductor (PMOS) transistor, and forming the dual-gate transistor of a second conductivity type as an n-channel metal oxide semiconductor (NMOS) transistor.

35. (Previously Presented) The method of claim 33, wherein the method further includes coupling a bit line to another gate of the dual-gate transistor in each inverter.

36. (Previously Presented) The method of claim 33, wherein the method further includes coupling an output transmission line to the drain region for the dual-gate transistor and the drain region of the transistor of the first conductivity type in each inverter. .

37. (Previously Presented) A method for forming a sense amplifier, comprising:

forming and cross coupling a pair of inverters, wherein forming and cross coupling each inverter includes:

forming a first transistor of a first conductivity type;

forming a dual-gate transistor of a second conductivity type, wherein forming the dual-gate transistor includes coupling the drain region for the dual-gate transistor to a drain region of the first transistor in each inverter, directly coupling the drain region for the dual-gate transistor in each inverter to a gate of the first transistor of the first conductivity type in the other inverter and to a gate of the dual-gate transistor of the second conductivity type in the other inverter, the dual-gated transistor having a threshold voltage ranging from about 0.3 V to about 0.35V;

coupling a bit line to another gate of the dual-gate transistor in each inverter, each bit line directly coupling the another gate of the dual-gate transistors in each inverter external to the sense amplifier; and

coupling an output transmission line to the drain region of the first transistor and to the drain region of the dual-gate transistor in each inverter.

38. (Previously Presented) The method of claim 37, wherein forming the first transistor of a first conductivity type includes forming a p-channel metal oxide semiconductor (PMOS) transistor, and wherein forming the dual-gate transistor of a second conductivity type includes forming an n-channel metal oxide semiconductor (NMOS) transistor.

39. (Cancelled)

40. (Previously Presented) A method for operating a sense amplifier, comprising:

equilibrating a first and second bit line, wherein the first bit line is coupled to a first gate of a dual-gate transistor in a first inverter in the sense amplifier and the second bit lines is coupled to a first gate of a dual-gate transistor in a second inverter in the sense amplifier, the first bit line directly coupling the first gate of the dual-gate transistor in the first inverter external to the sense amplifier and the second bit line directly coupling the first gate of the dual-gate

transistor in the second inverter external to the sense amplifier, the dual-gated transistor having a threshold voltage ranging from about 0.3 V to about 0.35V to operate in a sub-threshold or threshold region during most of switching transients of the dual-gated transistor;

discharging a memory cell onto the first bit line, wherein discharging a memory cell onto the first bit line drives a signal from a drain region for the first inverter directly to a gate of a PMOS transistor and to a second gate of a dual-gate transistor in the second inverter; and

providing a feedback from a drain region for the second inverter to a gate of a PMOS transistor and a second gate of a dual-gate transistor in the first inverter.

41. (Original) The method of claim 40, wherein operating the sense amplifier includes operating the sense amplifier with a power supply voltage of less that 1.0 Volts.

42. (Original) The method of claim 40, wherein operating the sense amplifier includes latching an output sense signal in less than 10 nanoseconds (ns).

43. (Original) The method of claim 40, wherein the method further includes removing the bit line capacitance from a pair of output nodes of the sense amplifier.

44. (Previously Presented) A method for operating a sense amplifier, comprising:

providing a first bit line signal directly from the external of the sense amplifier to a first gate of a dual-gate transistor in a first inverter of the sense amplifier, the dual-gated transistor having a threshold voltage ranging from about 0.3 V to about 0.35V to operate in a sub-threshold or threshold region during most of switching transients of the dual-gated transistor;

providing a second bit line signal directly from the external of the sense amplifier to a first gate of a dual-gate transistor in a second inverter of the sense amplifier

wherein providing the first and the second bit line signals to the first gates of the dual-gate transistors drives a signal directly from a drain region for the first inverter to a gate of a PMOS transistor and to a second gate of a dual-gate transistor in the second inverter; and

wherein providing the first and the second bit line signals to the first gates of the dual-gate transistors isolates the bit line capacitances from a first and second output node on the sense amplifier.

45. (Previously Presented) A method for operating a sense amplifier, comprising:

providing an input signal from a bit line directly from the external of the sense amplifier to a first gate of a dual-gate transistor in a first inverter of the sense amplifier, the dual-gated transistor having a threshold voltage ranging from about 0.3 V to about 0.35V to operate in a sub-threshold or threshold region during most of switching transients of the dual-gated transistor;

wherein providing the input signal from the bit line to the first gate of the dual-gate transistor in the first inverter of the sense amplifier drives a signal directly from a drain region for the first inverter to a gate of a PMOS transistor and to a gate of a dual-gate transistor in a second inverter; and

wherein providing the input signal to the first gate of the dual-gate transistor isolates the bit line capacitance from an output node on the sense amplifier.